

REMARKS

In an Office Action mailed on December 11, 2006, the Examiner: (1) rejected claims 11-24 and 26-34 under 35 U.S.C. § 103(a) based on a combination of Edwards (U.S. Pat. No. 6,484,683) and Steinberg et al. (U.S. Pat. No. 6,966,015); (2) rejected claim 25 under 35 U.S.C. § 103(a) based on a combination of Edwards and Steinberg et al. and further in view of Rohfleisch et al. (U.S. Pat. No. 7,058,855); (3) rejected claims 35-41 and 44 under 35 U.S.C. § 103(a) based on a combination of Steinberg et al. and Chen et al. (U.S. Pat. No. 5,642,478); (4) rejected claims 42 and 43 under 35 U.S.C. § 103(a) based on a combination of Steinberg et al. and Chen et al. and further in view of Rohfleisch et al.; and (5) rejected claim 45 under 35 U.S.C. 102(e) as being anticipated by Steinberg et al.

By this Amendment, Applicants cancel claims 35-45 without prejudice or disclaimer of the subject matter thereof.

Applicants respectfully request the Examiner to withdraw the rejection of pending claims 11-34 for at least the reasons given below. In a previously filed Amendment, Applicants had erroneously identified claims 11-34 as previously presented. The included listing of claims identifies these claims correctly as original.

Concerning the rejection of claims 11-24 and 26-34 under 35 U.S.C. § 103(a) based on a combination of Edwards and Steinberg et al., Applicants respectfully submit that the Examiner has failed to establish a prima facie case of obviousness. To establish a prima facie case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Third, the prior art reference (or references when combined) must teach or suggest all of the claim limitations. M.P.E.P. § 2143. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, not in applicant's disclosure. In re Vaeck, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991).

Applicants respectfully submit that the Examiner has failed to establish a prima facie case of obviousness for at least two reasons. First, the two references, even if combined, which they cannot be, fail to teach or suggest a plurality of functional circuit modules, each functional circuit module being clocked by a clock that represents a different time domain and having timestamping circuitry, the timestamping circuitry providing a message that indicates a point in time when a predetermined event occurs. The Examiner acknowledges that Edwards et al.

does not teach this limitation, and instead contends that Fig.2 and Fig. 3, element 44 of Steinberg et al. teach this limitation. Applicants respectfully disagree with the Examiner's conclusion for at least the following reasons.

In contrast to the subject matter of pending claims, Steinberg et al. is directed to improved techniques for reducing false alarms in network fault management systems. Apparently, these network fault management systems diagnose network problems before they happen by tracking correlation of certain network indicators based on a rule. In describing Figure 2, Steinberg et al. notes the problem with existing network fault management systems. Steinberg et al. states that an exemplary rule to diagnose a given problem involves analysis of three indicators identified as 1, 2, and 3, as shown in Figure 2. (col. 6, ll. 22-34). Each indicator may have two possible states: 0 and 1, with one state representing a severity condition and the other representing a normal operating condition. *Id.* Next, Steinberg et al. notes that if the rule to trigger an alarm provides that three indicators be collectively at a state of 1 for more than half the time, the correlation engine would generate an alert since in Figure 2 the rule would be satisfied. *Id.* Steinberg et al. then notes that while the rule is satisfied based on the states of the indicators in Figure 2, this might be a false alarm, since their concurrence may be caused by separate unconnected conditions. (col. 2, ll. 41-48).

To address this problem, Steinberg et al. proposes a scheme in which "the correlation engine 22 also includes an edge correlation routine 26 which improves the accuracy of rule-based correlation performed by the correlation engine 22 and reduces the number of false alarms generated by the engine 22." (col. 5, ll. 48-52). The edge correlation technique is what is explained with reference to Figure 3 and item 44. In particular, Steinberg et al. states that the "edge correlation routine compares the transitions of the indicators states over multiple discrete time periods for the monitored indicators, step 44." (col. 6, ll. 53-55). Apparently, this "analysis reveals the extent of coincidence of transitions of indicators during each time period, and is used to compute a transition correlation factor, step 46. (col. 6, ll. 56-58). This transition correlation factor is then used to modify the correlation factor to produce a new correlation factor, step 48. (col. 6, ll. 66-67). Thus, Steinberg et al. teaches the use of a transition correlation factor generated using an edge correlation routine to modify a prior art correlation factor used in network fault management systems. Steinberg et al., however, does not teach or suggest a plurality of functional circuit modules, each functional circuit module being clocked by a clock that represents a different time domain and having timestamping circuitry, the timestamping circuitry providing a message that indicates a point in time when a predetermined event occurs. Thus, because even the combined references fail to teach or suggest at least

one limitation of claims 11-24 and 26-34, the Examiner has failed to establish a prima facie case of obviousness with respect to claims 11-24 and 26-34.

Second, the Examiner has not provided any evidence of a motivation or suggestion to combine the two references. The Examiner states: “[o]ne of ordinary skill in the art at the time the invention would have been motivated to make the combination because Edwards discloses a debugging system for System-on-chip devices (Fig. 1) and Steinberg et al. discloses a method of correlating event data in different time slices (Fig. 1).” Applicants respectfully submit that by merely stating the problem that the two references are trying to solve does not motivate a person of ordinary skill in the art to combine the two references. Moreover, the two references are attempting to solve two unrelated problems. As explained above, unlike Edwards et al., Steinberg et al. is concerned with reducing false alarms generated by network fault management systems by using an edge correlation routine. That, however, would not motivate a person of ordinary skill in the art to combine Steinberg et al. with Edwards et al. Thus, for this additional reason, Applicants respectfully submit that the Examiner has failed to establish a prima facie case of obviousness. Accordingly, Applicants respectfully request the Examiner to withdraw the rejection of claims 11-24 and 26-34 under 35 U.S.C. § 103(a) based on a combination of Edwards and Steinberg et al.

Claim 25 depends from claim 24 and is thus patentable for at least the reasons given above with respect to claim 24.

Claims 35-45 have been canceled and thus their rejection is now moot. Applicants respectfully seek allowance of pending claims 11-34.

The Office Action contains numerous statements characterizing the claims, the Specification, and the prior art. Regardless of whether such statements are addressed by Applicants, Applicants refuse to subscribe to any of these statements, unless expressly indicated by Applicants. Should issues remain that might be subject to resolution through a telephonic interview, the Examiner is requested to telephone the undersigned at (512) 996-6839.

If Applicants have overlooked any additional fees, or if any overpayment has been made, the Commissioner is hereby authorized to credit or debit Deposit Account 503079, Freescale Semiconductor, Inc.

Respectfully submitted,

SEND CORRESPONDENCE TO:

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